REMARKS

This Amendment responds to the Final Office Action mailed May 23, 2006, and the Advisory Action mailed September 13, 2006, and supplements the Response mailed August 23, 2006. A Notice of Appeal was mailed on October 23, 2006, and was received by the Office on October 25, 2006. A Request for Continued Examination (RCE) accompanies this Amendment. Accordingly, entry of the Amendment and allowance of the application are respectfully requested.

Claims 1-6, 18 and 25-26 are pending in the application. By this Amendment, claims 1 and 18 are amended. No new matter has been added.

In reviewing the application, it was discovered that the previously pending claims did not accurately define the invention. In particular, it was not accurate to state that the first value, the second value, a result of the comparison and the trellis state metrics for time t_1 are determined in a single clock cycle, due to the pipelined structure of the digital signal processor. However, it is accurate to state that at least one trellis instruction is *completed* on each clock cycle of the digital signal processor when a series of trellis instructions are being processed. The error is regretted.

In the Final Office Action, the Examiner rejected claims 1 and 18 under 35 U.S.C. §102(b) as anticipated by Amon et al. (US 5,742,621). Claims 2-6, 25 and 26 were rejected under 35 U.S.C. §103(a) as unpatentable over Amon et al. in view of Benedetto et al. (article entitled "Soft-Output Decoding Algorithms in Iterative Decoding of Turbo Codes"). In previous Office Actions, the Examiner rejected claims 1 and 18 under 35 U.S.C. §103(a) as unpatentable over Amon et al. in view of Foland, Jr. (U.S. 5,412,669). The rejections are respectfully traversed in view of the amended claims.

Amon discloses a parallel data structure and a dedicated Viterbi specific shift left instruction for minimizing the number of clock cycles required for decoding a convolutionally encoded signal (col. 2, lines 10-14). However, Amon does not disclose or suggest a method for processing signal values wherein adding, subtracting, comparing and selection operations are

executed by a digital signal processor in response to *a single trellis instruction*, as required by amended claims 1 and 18. As explained below, Amon describes an add-compare-select butterfly operation that requires at least three instructions to perform adding, subtracting and comparing operations. The single trellis instruction of the present invention has the advantage that at least one trellis instruction, and thus the adding, subtracting, comparing and selecting operations, can be completed on each cycle of the pipelined digital signal processor during trellis processing. By contrast, the system of Amon requires at least three instructions to be completed for each add-compare-select operation. When data is being processed in real time, this difference can be very significant and can spell the difference between having sufficient computation speed to process the data and not having sufficient computation speed to process the data.

The Examiner asserts that the algorithm of Amon is executed in exactly three cycles, including add-compare-select operations in one cycle. Applicant must respectfully disagree.

FIG. 4 of Amon illustrates a first embodiment of assembly code for implementing the ACS butterfly (col. 9, lines 24-36). As shown in FIG. 4, an add instruction and a load instruction appear in the second code line of the main ACS loop; a subtract instruction appears in the third code line of the main ACS loop; and compare (MAX) and refetch instructions appear in the fourth code line of the main ACS loop. It is well established that assembly code is written with parallel operations in the same code line and sequential operations in sequential code lines. Thus, the add, subtract and compare instructions are separate instructions and are performed sequentially in different clock cycles. This interpretation is supported at col. 9, lines 30 and 31, where it is stated that one loop of the ACS butterfly is completed in 14 clock cycles. A loop execution time of 14 clock cycles is inconsistent with performing each of two instances of add, subtract and compare operations in a single clock cycle. Instead, Amon clearly teaches that three instructions are utilized to perform the add, subtract and compare operations.

FIG. 5 of Amon illustrates a second embodiment of assembly code for implementing the ACS butterfly (col. 9, lines 37-49). Similarly to FIG. 4, separate add, subtract and compare instructions appear on second, third and fourth code lines, respectively, of the main ACS loop.

Amon states at col. 9, lines 45-46 that the assembly code of FIG. 5 permits one loop of the ACS butterfly to be performed in 10 clock cycles. Again, a loop execution time of 10 clock cycles is inconsistent with performing each of two instances of add, subtract and compare operations in a single clock cycle. Further, FIG. 5 clearly teaches that three instructions are used to perform add, subtract and compare operations.

Claim 7 of the Amon patent recites the steps of: (a) fetching during a first single clock cycle; (b) fetching during a second single clock cycle; (c) adding; (d) subtracting; (e) comparing, selecting and refetching during a third single clock cycle; (f) storing; etc. The adding, subtracting and comparing steps appear in separate paragraphs of claim 7. This is fully consistent with the assembly code shown in FIGs. 4 and 5 and with the interpretation that the first, second and third single clock cycles recited in these claims are not consecutive clock cycles. Applicant submits that one of ordinary skill in the art would read claim 7 of Amon, as well as the remainder of the Amon patent, as requiring only the comparing, selecting and refetching operations of step (e) to be performed in a single clock cycle and not as requiring the adding, subtracting and comparing operations of steps (c), (d) and (e) to be performed in a single clock cycle. The language of claim 7 describes operations that occur during three single clock cycles, but those clock cycles are not consecutive clock cycles.

In summary, Amon does not teach or suggest a method or processor for processing signal values wherein adding, subtracting, comparing and selecting operations are executed by a processor in response to a single trellis instruction, as required by Applicants' amended claims 1 and 18. Accordingly, claims 1 and 18 are clearly and patentably distinguished over Amon, and withdrawal of the rejection is respectfully requested.

Foland, Jr. does not provide the teachings that are lacking in Amon. The Foland, Jr. patent describes an add-compare-select circuit used with magnetic recording equipment. However, Foland, Jr. does not describe a programmable processor and does not disclose or suggest a single trellis instruction that specifies trellis state metrics and transition metrics and which causes adding, subtracting, comparing and selecting operations to be executed by a

programmable processor in response to a single trellis instruction, as required by Applicants' claims.

Based upon the above discussion, amended claims 1 and 18 are clearly and patentably distinguished over Amon, taken alone or in combination with Foland, Jr. Claims 2-6 depend from claim 1, and claims 25 and 26 depend from claim 18. Claims 2-6, 25 and 26 are patentable over the cited references for at least the same reasons as claims 1 and 18.

Based upon the above discussion, claims 1-6, 18, 25 and 26 are in condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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